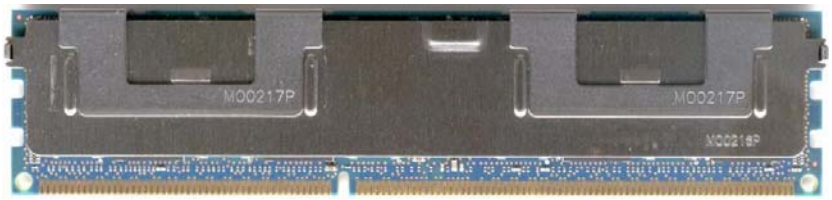
DTM64330A

8GB - 240-Pin 4Rx8 Registered ECC DDR3 DIMM



Identification

DTM64330A 1Gx72
8GB 4Rx8 PC3-8500R-7-10-H0

Performance range

Clock / Module Speed / CL-t_{RCD} -t_{RP}

533 MHz / PC3-8500 / 8-8-8
533 MHz / PC3-8500 / 7-7-7
400 MHz / PC3-6400 / 6-6-6

Features

- 240-pin JEDEC-compliant DIMM, 133.35 mm wide by 30 mm high
- Operating Voltage: 1.5V ±0.075
- I/O Type: SSTL_15
- On-board I^2C temperature sensor with integrated Serial Presence-Detect (SPD) EEPROM
- Data Transfer Rate: 8.5 Gigabytes/sec
- Data Bursts: 8 and burst chop 4 mode
- ZQ Calibration for Output Driver and On-Die Termination (ODT)
- Programmable ODT / Dynamic ODT during Writes
- Programmable CAS Latency: 6, 7, and 8
- Bi-directional Differential Data Strobe signals
- SDRAM Addressing (Row/Col/Bank): 15/10/3
- Fully RoHS Compliant

Description

DTM64330A is a registered 1Gx72 memory module, which conforms to JEDEC's DDR3, PC3-8500 standard. The assembly is Quad-Rank. Each Rank is comprised of nine 256Mx8 DDR3 Hynix SDRAMs. One 2K-bit EEPROM is used for Serial Presence Detect and a combination register/PLL, with Address and Command Parity, is also used.

Both output driver strength and input termination impedance are programmable to maintain signal integrity on the I/O signals in a Fly-by topology. A thermal sensor accurately monitors the DIMM module and can prevent exceeding the maximum operating temperature of 95C. A Heat Spreader is attached to improve the thermal characteristics of the module.

Pin Configuration

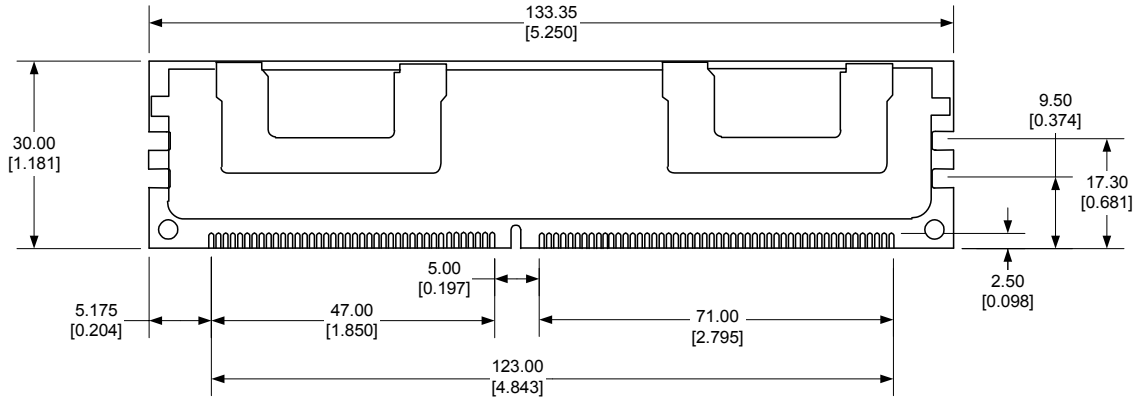
Front Side								Back Side							
1	V_{REFDQ}	31	DQ25	61	A2	91	DQ41	121	V_{SS}	151	V_{SS}	181	A1	211	V_{SS}
2	V_{SS}	32	V_{SS}	62	V_{DD}	92	V_{SS}	122	DQ4	152	DM3	182	V_{DD}	212	DM5
3	DQ0	33	/DQS3	63	CK1*	93	/DQS5	123	DQ5	153	/ TDQS12	183	V_{DD}	213	/ TDQS14
4	DQ1	34	DQS3	64	/CK1*	94	DQS5	124	V_{SS}	154	V_{SS}	184	CK0	214	V_{SS}
5	V_{SS}	35	V_{SS}	65	V_{DD}	95	V_{SS}	125	DM0	155	DQ30	185	/CK0	215	DQ46
6	/DQS0	36	DQ26	66	V_{DD}	96	DQ42	126	/TDQS9	156	DQ31	186	V_{DD}	216	DQ47
7	DQS0	37	DQ27	67	V_{REFCA}	97	DQ43	127	V_{SS}	157	V_{SS}	187	/Event	217	V_{SS}
8	V_{SS}	38	V_{SS}	68	P_{AR_IN}	98	V_{SS}	128	DQ6	158	CB4	188	A0	218	DQ52
9	DQ2	39	CB0	69	VDD	99	DQ48	129	DQ7	159	CB5	189	V_{DD}	219	DQ53
10	DQ3	40	CB1	70	A10/AP	100	DQ49	130	V_{SS}	160	V_{SS}	190	BA1	220	V_{SS}
11	V_{SS}	41	V_{SS}	71	BA0	101	V_{SS}	131	DQ12	161	DM8	191	V_{DD}	221	DM6
12	DQ8	42	/DQS8	72	V_{DD}	102	/DQS6	132	DQ13	162	/ TDQS17	192	/RAS	222	/ TDQS15
13	DQ9	43	DQS8	73	/WE	103	DQS6	133	V_{SS}	163	V_{SS}	193	/S0	223	V_{SS}
14	V_{SS}	44	V_{SS}	74	/CAS	104	V_{SS}	134	DM1	164	CB6	194	V_{DD}	224	DQ54
15	/DQS1	45	CB2	75	V_{DD}	105	DQ50	135	/ TDQS10	165	CB7	195	ODT0	225	DQ55
16	DQS1	46	CB3	76	/S1	106	DQ51	136	V_{SS}	166	V_{SS}	196	A13	226	V_{SS}
17	V_{SS}	47	V_{SS}	77	ODT1	107	V_{SS}	137	DQ14	167	NC (TEST)	197	V_{DD}	227	DQ60
18	DQ10	48	V_{TT}	78	V_{DD}	108	DQ56	138	DQ15	168	/RESET	198	/S3	228	DQ61
19	DQ11	49	V_{TT}	79	/S2	109	DQ57	139	V_{SS}	169	CKE1	199	V_{SS}	229	V_{SS}
20	V_{SS}	50	CKE0	80	V_{SS}	110	V_{SS}	140	DQ20	170	V_{DD}	200	DQ36	230	DM7
21	DQ16	51	V_{DD}	81	DQ32	111	/DQS7	141	DQ21	171	A15	201	DQ37	231	/ TDQS16
22	DQ17	52	BA2	82	DQ33	112	DQS7	142	V_{SS}	172	A14	202	V_{SS}	232	V_{SS}
23	V_{SS}	53	$/E_{RR}\_O_{UT}$	83	V_{SS}	113	V_{SS}	143	DM2	173	V_{DD}	203	DM4	233	DQ62
24	/DQS2	54	V_{DD}	84	/DQS4	114	DQ58	144	/ TDQS11	174	A12/ /BC	204	/TDQS13	234	DQ63
25	DQS2	55	A11	85	DQS4	115	DQ59	145	V_{SS}	175	A9	205	V_{SS}	235	V_{SS}
26	V_{SS}	56	A7	86	V_{SS}	116	V_{SS}	146	DQ22	176	V_{DD}	206	DQ38	236	V_{DDSPD}
27	DQ18	57	V_{DD}	87	DQ34	117	SA0	147	DQ23	177	A8	207	DQ39	237	SA1
28	DQ19	58	A5	88	DQ35	118	SCL	148	V_{SS}	178	A6	208	V_{SS}	238	SDA
29	V_{SS}	59	A4	89	V_{SS}	119	SA2	149	DQ28	179	V_{DD}	209	DQ44	239	V_{SS}
30	DQ24	60	V_{DD}	90	DQ40	120	V_{TT}	150	DQ29	180	A3	210	DQ45	240	V_{TT}

* Not used

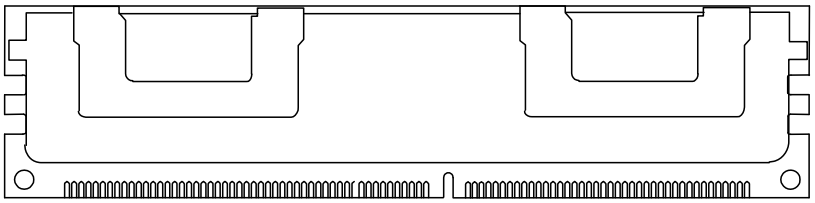
Pin Description

Name	Function
CB[7:0]	Data Check Bits
DQ[63:0]	Data Bits
DQS[8:0], /DQS[8:0]	Differential Data Strobes
DM[8:0]	Data Mask
/TDQS[17:9]	Termination Data Strobes
CK[1:0], /CK[1:0]	Differential Clock Inputs
CKE[1:0]	Clock Enables
/CAS	Column Address Strobe
/RAS	Row Address Strobe
/S[3:0]	Chip Selects
/WE	Write Enable
A[15:0]	Address Inputs
BA[2:0]	Bank Addresses
ODT[1:0]	On Die Termination Inputs
SA[2:0]	SPD Address
SCL	SPD Clock Input
SDA	SPD Data Input/Output
V_{SS}	Ground
V_{DD}	Power
V_{DDSPD}	SPD EEPROM Power
V_{REFDQ}	Reference Voltage for DQ
V_{REFCA}	Reference Voltage for CA
V_{TT}	Termination Voltage
/Event	Temperature Sensing
NC	No Connection

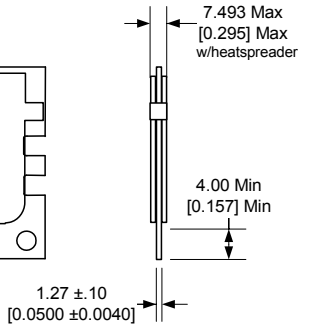
Front view



Back view



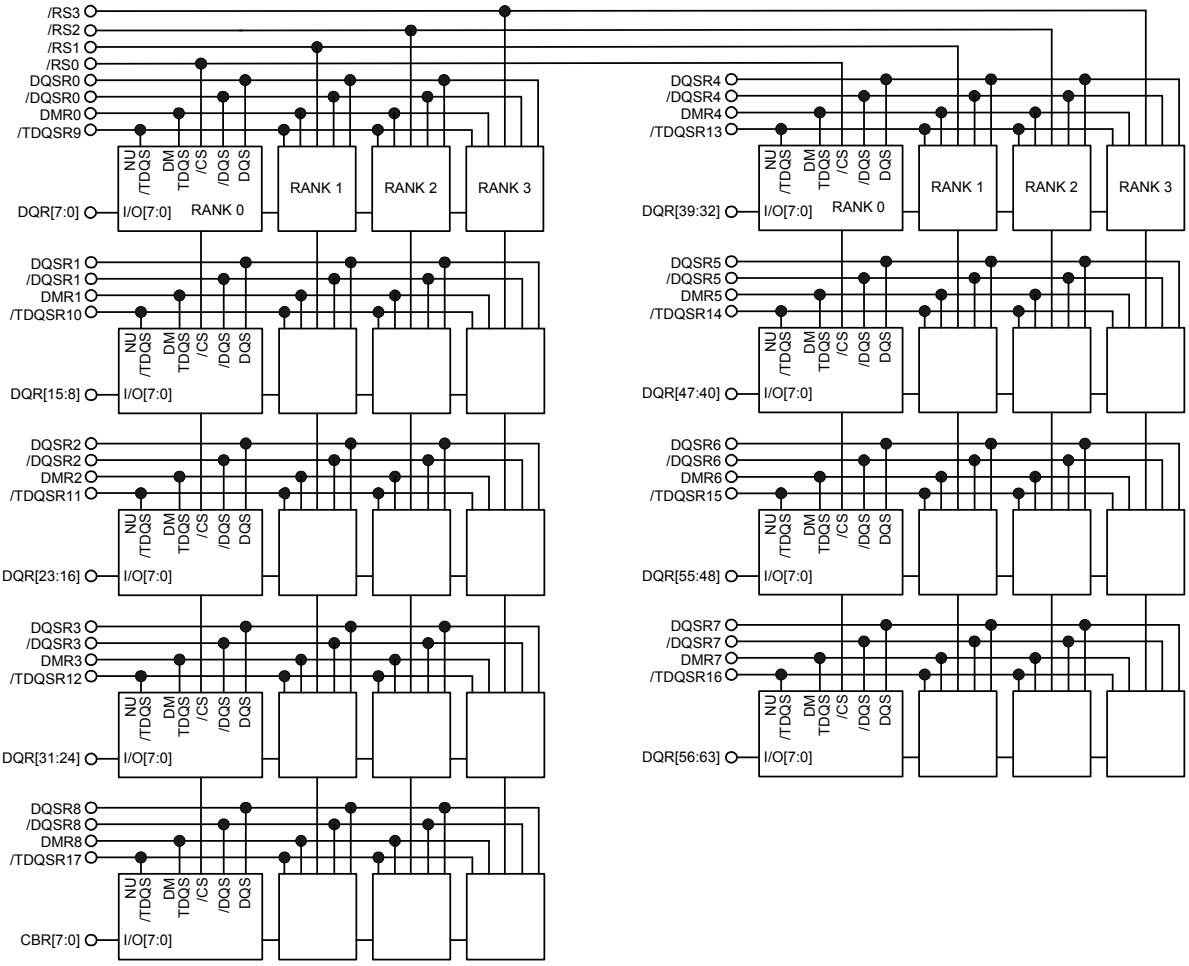
Side view

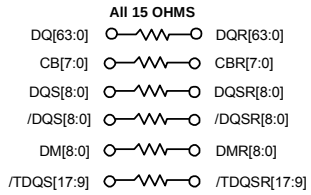


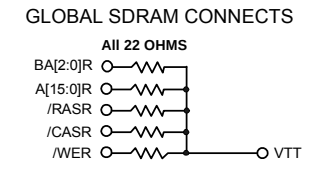
Notes

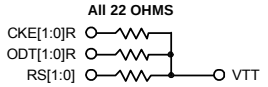
Tolerances on all dimensions except where otherwise indicated are ±.13 (.005).

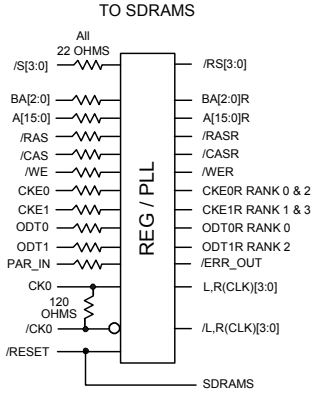
All dimensions are expressed: millimeters [inches]

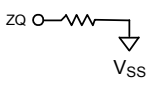

/RS3
/RS2
/RS1
/RS0
DQSR0
/DQSR0
DMR0
/TDQSR9
DQR[7:0]
I/O[7:0]
RANK 0
RANK 1
RANK 2
RANK 3
NU /TDQS
DM TDQS
/CS
/DQS
DQS
DQSR1
/DQSR1
DMR1
/TDQSR10
DQR[15:8]
DQSR2
/DQSR2
DMR2
/TDQSR11
DQR[23:16]
DQSR3
/DQSR3
DMR3
/TDQSR12
DQR[31:24]
DQSR8
/DQSR8
DMR8
/TDQSR17
CBR[7:0]
DQSR4
/DQSR4
DMR4
/TDQSR13
DQR[39:32]
DQSR5
/DQSR5
DMR5
/TDQSR14
DQR[47:40]
DQSR6
/DQSR6
DMR6
/TDQSR15
DQR[55:48]
DQSR7
/DQSR7
DMR7
/TDQSR16
DQR[56:63]

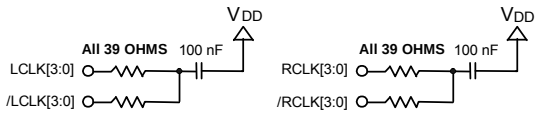

All 15 OHMS
DQ[63:0]
DQR[63:0]
CB[7:0]
CBR[7:0]
DQS[8:0]
DQSR[8:0]
/DQS[8:0]
/DQSR[8:0]
DM[8:0]
DMR[8:0]
/TDQS[17:9]
/TDQSR[17:9]

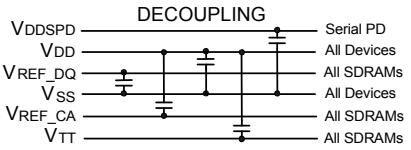

GLOBAL SDRAM CONNECTS
All 22 OHMS
BA[2:0]R
A[15:0]R
/RASR
/CASR
/WER
VTT

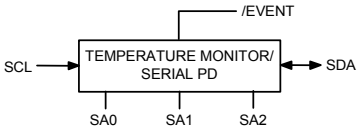

All 22 OHMS
CKE[1:0]R
ODT[1:0]R
RS[1:0]
VTT


TO SDRAMS
All 22 OHMS
/S[3:0]
BA[2:0]
A[15:0]
/RAS
/CAS
/WE
CKE0
CKE1
ODT0
ODT1
PAR_IN
CK0
120 OHMS
/CK0
/RESET
REG / PLL
/RS[3:0]
BA[2:0]R
A[15:0]R
/RASR
/CASR
/WER
CKE0R RANK 0 & 2
CKE1R RANK 1 & 3
ODT0R RANK 0
ODT1R RANK 2
/ERR_OUT
L,R(CLK)[3:0]
/L,R(CLK)[3:0]
SDRAMS


All 240 OHMS
ZQ
VSS


VDD
All 39 OHMS
100 nF
LCLK[3:0]
/LCLK[3:0]
VDD
All 39 OHMS
100 nF
RCLK[3:0]
/RCLK[3:0]


DECOUPLING
VDDSPD
VDD
VREF_DQ
VSS
VREF_CA
VTT
Serial PD
All Devices
All SDRAMs
All Devices
All SDRAMs
All SDRAMs


/EVENT
SCL
TEMPERATURE MONITOR/
SERIAL PD
SDA
SA0
SA1
SA2

Absolute Maximum Ratings

(Note: Operation at or above Absolute Maximum Ratings can adversely affect module reliability.)

PARAMETER	Symbol	Minimum	Maximum	Unit
Temperature, non-Operating	$T_{STORAGE}$	-55	100	C
Ambient Temperature, Operating	T_A	0	70	C
DRAM Case Temperature, Operating	T_{CASE}	0	95	C
Voltage on V_{DD} relative to V_{SS}	V_{DD}	-0.4	1.975	V
Voltage on Any Pin relative to V_{SS}	V_{IN},V_{OUT}	-0.4	1.975	V

Notes:

DRAM Operating Case Temperature above 85C requires 2X refresh.

Recommended DC Operating Conditions (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Minimum	Typical	Maximum	Unit	Note
Power Supply Voltage	V_{DD}	1.425	1.5	1.575	V	
I/O Reference Voltage	V_{REFDQ}	0.49 V_{DD}	0.50 V_{DD}	0.51 V_{DD}	V	1
I/O Reference Voltage	V_{REFCA}	0.49 V_{DD}	0.50 V_{DD}	0.51 V_{DD}	V	1

Notes:

1) The value of V_{REF} is expected to equal one-half V_{DD} and to track variations in the V_{DD} DC level. Peak-to-peak noise on V_{REF} may not exceed ±1% of its DC value.

DC Input Logic Levels, Single-Ended (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Minimum	Maximum	Unit
Logical High (Logic 1)	$V_{IH(DC)}$	V_{REF} + 0.1	V_{DD}	V
Logical Low (Logic 0)	$V_{IL(DC)}$	V_{SS}	V_{REF} - 0.1	V

AC Input Logic Levels, Single-Ended (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Minimum	Maximum	Unit
Logical High (Logic 1)	$V_{IH(AC)}$	V_{REF} + 0.175	-	V
Logical Low (Logic 0)	$V_{IL(AC)}$	-	V_{REF} - 0.175	V

Differential Input Logic Levels (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Minimum	Maximum	Unit
Differential Input Logic High	$V_{IH.DIFF}$	+0.200	DC:V_{DD} AC:V_{DD}+0.4	V
Differential Input Logic Low	$V_{IL.DIFF}$	DC:V_{SS} AC:V_{SS}-0.4	-0.200	V
Differential Input Cross Point Voltage relative to VDD/2	V_{IX}	- 0.150	+ 0.150	V

Capacitance (T_A = 25 C, f = 100 MHz)

PARAMETER	Pin	Symbol	Minimum	Maximum	Unit
Input Capacitance, Clock	CK0, /CK0	C_{CK}	1.5	2.5	pF
Input Capacitance, Address	BA[2:0], A[15:0], /RAS, /CAS, /WE	C_I	1.5	2.5	pF
Input Capacitance Control	/S[3:0], CKE[1:0], ODT[1:0]	C_I	1.5	2.5	pF
Input/Output Capacitance	DQ[63:0], CB[7:0] DQS[8:0], /DQS[8:0], DM[8:0], /TDQS[17:9]	C_{IO}	6	10	pF

DC Characteristics (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Minimum	Maximum	Unit	Note
Input Leakage Current (Any input 0 V < VIN < VDD)	I_{IL}	-18	+18	µA	1,2
Output Leakage Current (0V < VOUT < VDDQ)	I_{OL}	-10	+10	µA	2,3

Notes:
1) All other pins not under test = 0 V
2) Values are shown per pin
3) DQ, DQS, DQS and ODT are disabled

I_{DD} Specifications and Conditions (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Test Condition	Max Value	Unit
Operating One Bank Active-Precharge Current	$I_{DD}0$*	Operating current : One bank ACTIVATE-to-PRECHARGE	999	mA
Operating One Bank Active-Read-Precharge Current	$I_{DD}1$*	Operating current : One bank ACTIVATE-to-READ-to-PRECHARGE	1089	mA
Precharge Power-Down Current	$I_{DD}2P$**	Precharge power down current: (Slow exit)	432	mA
Precharge Power-Down Current	$I_{DD}2P$**	Precharge power down current: (Fast exit)	1080	mA
Precharge Standby Current	$I_{DD}2N$**	Precharge standby current	1620	mA
Active Power-Down Current	$I_{DD}3P$**	Active power-down current	1260	mA
Active Standby Current	$I_{DD}3N$**	Active standby current	1980	mA
Operating Burst Write Current	$I_{DD}4W$*	Burst write operating current	1629	mA
Operating Burst Read Current	$I_{DD}4R$*	Burst read operating current	1584	mA
Burst Refresh Current	$I_{DD}5B$**	Refresh current	7560	mA
Self Refresh Current	$I_{DD}6$**	Self-refresh temperature current: MAX T_C = 85°C	432	mA
Operating Bank Interleave Read Current	$I_{DD}7$*	All bank interleaved read current	2214	mA

* One module rank in this operation, the rest in IDD2P slow exit.
** All module ranks in this operation.

AC Operating Conditions

PARAMETER	Symbol	Min	Max	Unit
Internal read command to first data	t_{AA}	13.125	20	ns
CAS-to-CAS Command Delay	t_{CCD}	4	-	t_{CK}
Clock High Level Width	$t_{CH(avg)}$	0.47	0.53	t_{CK}
Clock Cycle Time	t_{CK}	1.875	2.500	ns
Clock Low Level Width	$t_{CL(avg)}$	0.47	0.53	t_{CK}
Data Input Hold Time after DQS Strobe	t_{DH}	100	-	ps
DQ Input Pulse Width	t_{DIPW}	490	-	ps
DQS Output Access Time from Clock	t_{DQSCK}	-300	+300	ps
Write DQS High Level Width	t_{DQSH}	0.45	0.55	$t_{CK(avg)}$
Write DQS Low Level Width	t_{DQSL}	0.45	0.55	$t_{CK(avg)}$
DQS-Out Edge to Data-Out Edge Skew	t_{DQSQ}	-	150	ps
Data Input Setup Time Before DQS Strobe	t_{DS}	25	-	ps
DQS Falling Edge from Clock, Hold Time	t_{DSH}	0.2	-	$t_{CK(avg)}$
DQS Falling Edge to Clock, Setup Time	t_{DSS}	0.2	-	$t_{CK(avg)}$
Address and Command Hold Time after Clock	t_{IH}	200	-	ps
Address and Command Setup Time before Clock	t_{IS}	125	-	ps
Load Mode Command Cycle Time	t_{MRD}	4	-	t_{CK}
DQ-to-DQS Hold	t_{QH}	0.38	-	$t_{CK(avg)}$
Active-to-Precharge Time	t_{RAS}	37.5	$9*t_{REFI}$	ns
Active-to-Active / Auto Refresh Time	t_{RC}	50.625	-	ns
RAS-to-CAS Delay	t_{RCD}	13.125	-	ns
Average Periodic Refresh Interval $0^o C \leq T_{CASE} < 85^o C$	t_{REFI}	-	7.8	µs
Average Periodic Refresh Interval $85^o C \leq T_{CASE} < 95^o C$	t_{REFI}	-	3.9	µs
Auto Refresh Row Cycle Time	t_{RFC}	160	-	ns
Row Precharge Time	t_{RP}	13.125	-	ns
Read DQS Preamble Time	t_{RPRE}	0.9	Note 1	$t_{CK(avg)}$
Read DQS Postamble Time	t_{RPST}	0.3	Note 2	$t_{CK(avg)}$
Row Active to Row Active Delay	t_{RRD}	Max(4nCK, 7.5ns)	-	ns
Internal Read to Precharge Command Delay	t_{RTP}	Max(4nCK, 7.5ns)	-	ns
Write DQS Preamble Setup Time	t_{WPRE}	0.9	-	$t_{CK(avg)}$
Write DQS Postamble Time	t_{WPST}	0.3	-	$t_{CK(avg)}$
Write Recovery Time	t_{WR}	15	-	ns
Internal Write to Read Command Delay	t_{WTR}	Max(4nCK, 7.5ns)	-	ns

Notes:
1. The maximum preamble is bound by tLZDQS(min)
2. The maximum postamble is bound by tHZDQS(max)

SERIAL PRESENCE DETECT MATRIX

Byte#	Function.	Value	Hex
0	Number of Bytes Used / Number of Bytes in SPD Device / CRC Coverage.		0x92
	Bit 3 ~ Bit 0. SPD Bytes Used -	176	
	Bit 6 ~ Bit 4. SPD Bytes Total -	256	
	Bit 7. CRC Coverage -	Bytes 0-116	
1	SPD Revision.	Rev. 1.0	0x10
2	Key Byte / DRAM Device Type.	DDR3 SDRAM	0x0B
3	Key Byte / Module Type.		0x01
	Bit 3 ~ Bit 0. Module Type -	RDIMM	
	Bit 7 ~ Bit 4. Reserved -	0	
4	SDRAM Density and Banks.		0x03
	Bit 3 ~ Bit 0. Total SDRAM capacity, in megabits -	2Gb	
	Bit 6 ~ Bit 4. Bank Address Bits -	8 banks	
	Bit 7. Reserved -	0	
5	SDRAM Addressing.		0x19
	Bit 2 ~ Bit 0. Column Address Bits -	10	
	Bit 5 ~ Bit 3. Row Address Bits -	15	
	Bit 7, 6. Reserved	0	
6	Reserved.	UNUSED	0x00
7	Module Organization.		0x19
	Bit 2 ~ Bit 0. SDRAM Device Width -	8-Bits	
	Bit 5 ~ Bit 3. Number of Ranks -	4-Rank	
	Bit 7, 6. Reserved	0	
8	Module Memory Bus Width.		0x0B
	Bit 2 ~ Bit 0. Primary bus width, in bits -	64-Bits	
	Bit 4, Bit 3. Bus width extension, in bits -	8-Bits	
	Bit 7 ~ Bit 5. Reserved -	0	
9	Fine Timebase (FTB) Dividend / Divisor.		0x52
	Bit 3 ~ Bit 0. Fine Timebase (FTB) Divisor	2	
	Bit 7 ~ Bit 4. Fine Timebase (FTB) Dividend	5	
10	Medium Timebase (MTB) Dividend.	1 (MTB = 0.125ns)	0x01
11	Medium Timebase (MTB) Divisor.	8 (MTB = 0.125ns)	0x08
12	SDRAM Minimum Cycle Time (tCKmin).	1.875ns	0x0F
13	Reserved.	UNUSED	0x00
14	CAS Latencies Supported, Least Significant Byte.		0x1C
	Bit 0. CL = 4 -		
	Bit 1. CL = 5 -		
	Bit 2. CL = 6 -	X	
	Bit 3. CL = 7 -	X	
	Bit 4. CL = 8 -	X	

	Bit 5. CL = 9 -		
	Bit 6. CL = 10 -		
	Bit 7. CL = 11 -		
15	CAS Latencies Supported, Most Significant Byte.		0x00
	Bit 0. CL = 12 -		
	Bit 1. CL = 13 -		
	Bit 2. CL =14 -		
	Bit 3. CL = 15 -		
	Bit 4. CL = 16 -		
	Bit 5. CL = 17 -		
	Bit 6. CL = 18 -		
	Bit 7. Reserved.		
16	Minimum CAS Latency Time (tAAmin).	13.125ns	0x69
17	Minimum Write Recovery Time (tWRmin).	15.0ns	0x78
18	Minimum RAS# to CAS# Delay Time (tRCDmin).	13.125ns	0x69
19	Minimum Row Active to Row Active Delay Time (tRRDmin).	7.5ns	0x3C
20	Minimum Row Precharge Delay Time (tRPmin).	13.125ns	0x69
21	Upper Nibbles for tRAS and tRC.		0x11
	Bit 3 ~ Bit 0. tRAS Most Significant Nibble -	1	
	Bit 7 ~ Bit 4. tRC Most Significant Nibble -	1	
22	Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte.	37.5ns	0x2C
23	Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte.	50.625ns	0x95
24	Minimum Refresh Recovery Delay Time (tRFCmin), Least Significant Byte.	160.0ns	0x00
25	Minimum Refresh Recovery Delay Time (tRFCmin), Most Significant Byte.		0x05
26	Minimum Internal Write to Read Command Delay Time (tWTRmin).	7.5ns	0x3C
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin).	7.5ns	0x3C
28	Upper Nibble for tFAW.		0x01
	Bit 3 ~ Bit 0. tFAW Most Significant Nibble -	1	
	Bit 7 ~ Bit 4. Reserved -	0	
29	Minimum Four Activate Window Delay Time (tFAWmin), Least Significant Byte.	37.5	0x2C
30	SDRAM Optional Features.		0x83
	Bit 0. RZQ / 6 -	X	
	Bit 1. RZQ / 7 -	X	
	Bit 6 ~ Bit 2. Reserved -		
	Bit 7. DLL-Off Mode Support		
31	SDRAM Drivers Supported.		0x05
	Extended Temperature Range -	X	
	Extended Temperature Refresh Rate with standard 1X refresh rate -		
	Auto Self Refresh (ASR) -	X	
	On-die Thermal Sensor (ODTS) Readout -		
	Reserved -		
	Reserved -		
	Reserved -		

	Reserved -		
32	Reserved		0x80
33-59	Reserved	UNUSED	0x00
60	Module Nominal Height.		0x10
	Bit 4 ~ Bit 0. Module Nominal Height max, in mm -	30<h<=31	
	Bit 7 ~ Bit5. Reserved -	0	
61	Module Maximum Thickness.		0x22
	Bit 3 ~ Bit 0. Front, in mm (baseline thickness = 1 mm) -	2<th<=3	
	Bit 7 ~ Bit 4. Back, in mm (baseline thickness = 1 mm) -	2<th<=3	
62	Reference Raw Card Used.		0x07
	Bit 4 ~ Bit 0. Reference Raw Card -	R/C H	
	Bit 6, Bit 5. Reference Raw Card Revision -	Rev.0	
	Bit 7. Reserved -	0	
63	DIMM Module Attributes.		0x09
	Bit 1, Bit 0. # of Registers used on RDIMM -	1	
	Bit 3, Bit 2. # of Rows of DRAMs on RDIMM -	2	
	Bit 7 ~ Bit 1. Reserved -		
64	Module-Specific Section		0x80
65	Module-Specific Section		0x00
66	Module-Specific Section		0x00
67	Module-Specific Section		0xFF
68,69	Module-Specific Section	UNUSED	0x00
70	Module-Specific Section		0x50
71	Module-Specific Section		0x55
72-112	Module-Specific Section	UNUSED	0x00
113	Module-Specific Section.	UNUSED	0x00
114-116	Module-Specific Section	UNUSED	0x00
117	Module Manufacturer ID Code, Least Significant Byte		0x01
118	Module Manufacturer ID Code, Most Significant Byte		0x91
119	Module Manufacturing Location	UNUSED	0x00
120,121	Module Manufacturing Date		0x20
122-125	Module Serial Number		0x20
126	Cyclical Redundancy Code (CRC).	CRC	0x6E
127	Cyclical Redundancy Code (CRC).	CRC	0xA9
128-131	Module Part Number		0x20
132	Module Part Number	D	0x44
133	Module Part Number	A	0x41
134	Module Part Number	T	0x54
135	Module Part Number	A	0x41
136	Module Part Number	R	0x52
137	Module Part Number	A	0x41
138	Module Part Number	M	0x4D
139	Module Part Number		0x20
140	Module Part Number	6	0x36
141	Module Part Number	4	0x34

142	Module Part Number	3	0x33
143	Module Part Number	3	0x33
144	Module Part Number	0	0x30
145	Module Part Number		0x20
146,147	Module Revision Code		0x20
148	DRAM Manufacturer ID Code, Least Significant Byte	UNUSED	0x00
149	DRAM Manufacturer ID Code, Most Significant Byte	UNUSED	0x00
150-175	Manufacturer's Specific Data	UNUSED	0x00
176-255	Open for customer use	UNUSED	0x00

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